

CLAIMS

- 1 1. A memory package comprising:
  - 2 a first circuit board having two faces, the first circuit board comprising a memory
  - 3 die on a first face of the circuit board and a controller die on the second face;
  - 4 a second circuit board having two faces and an opening, the first face of the
  - 5 second circuit board affixed to the second face of the first circuit board such that the
  - 6 controller die is within the opening; and
  - 7 vias connecting the memory die to the second face of the second circuit board,
  - 8 and connecting the memory die to the controller die.
- 1 2. The memory package of claim 1 further comprising solder balls on the second
- 2 face of the second circuit board, the solder balls affixed to the vias.
- 1 3. The memory package of claim 1 further comprising a first encapsulant covering
- 2 the memory die and a portion of the first circuit board.
- 1 4. The memory package of claim 1 further comprising a second encapsulant
- 2 covering the controller die.
- 1 5. The memory package of claim 1 wherein the thickness of the package is about 0.7
- 2 millimeters.
- 1 6. The memory package of claim 2, wherein the thickness of the package including
- 2 the solder balls is about 1.0 millimeters.
- 1 7. The memory package of claim 1 further comprising bond wires, the bond wires
- 2 connecting the memory die and the controller die to the vias or a conductive layer of the
- 3 first circuit board coupled to the vias.
- 1 8. The memory package of claim 1, wherein the memory die is conductively affixed
- 2 to a conductive layer of the first circuit board without the use of bond wires.

- 1 9. The memory package of claim 1, wherein the controller die is conductively  
2 affixed to a conductive layer of the first circuit board without the use of bond wires.
- 1 10. The memory package of claim 1, wherein the memory is FLASH type memory.
- 1 11. The memory package of claim 1 further comprising a set of contacts on either the  
2 first or second circuit board, the set of contacts exposed.
- 1 12. A memory package comprising:  
2 a circuit board having a first and second face, the second face having a recess;  
3 a memory die attached to the first face of the circuit board, the memory die  
4 positioned above the recess;  
5 a controller die attached to and positioned within the recess of the second face of  
6 the circuit board, the second face of the circuit board forming a second face of the  
7 package; and  
8 vias connecting the memory die to the second face of the circuit board.
- 1 13. The memory package of claim 12 further comprising bond wires, the bond wires  
2 connecting the memory die and the controller die to the vias or a conductive layer of the  
3 circuit board coupled to the vias.
- 1 14. The memory package of claim 12, wherein the memory die is conductively  
2 affixed to a conductive layer of the circuit board without the use of bond wires.
- 1 15. The memory package of claim 12, wherein the controller die is conductively  
2 affixed to a conductive layer of the circuit board without the use of bond wires.
- 1 16. The memory package of claim 12, wherein the memory is FLASH type memory.
- 1 17. The memory package of claim 12 further comprising a set of contacts on a face of  
2 the circuit board.
- 1 18. The memory package of claim 17 wherein the contacts are on the second face of  
2 the circuit board.

1 19. The memory package of claim 17 further comprising an encapsulent around the  
2 first face and edges of the package.

1 20. The memory package of claim 18, further comprising a plastic covering over the  
2 first and second face and the edges of the package.

1 21. A method of making a memory package comprising:

2 attaching a plurality of memory die to the first face of a first circuit board;

3 attaching a plurality of controller die to the second face of the first circuit board,  
4 each controller die positioned beneath a memory die;

5 laminating the second face of the first circuit board to a first face of a second  
6 circuit board having a plurality of recesses such that the plurality of controller die fit  
7 within the plurality of recesses;

8 forming vias in the first and second circuit boards connecting the controller die to  
9 beneath the memory die to the memory die to form a plurality of memory packages; and

10 cutting the first and second circuit boards between the plurality of memory  
11 packages to form individual memory packages.

1 22. A memory card comprising:

2 a first circuit board having a first and second face;

3 a memory package comprising a second circuit board, a controller die attached to  
4 a first face of the second circuit board, and a memory die attached to a second face of the  
5 second circuit board, and wherein

6 the memory package is attached to the first face of the first circuit board; and

7 a set of contacts on the second face of the first circuit board.

1 23. The memory card of claim 22 further comprising a set of circuit traces within the  
2 first circuit board coupled to the memory die, controller die, and the set of contacts.

1 24. The memory card of claim 23 wherein the circuit traces are coupled to the  
2 memory die, controller die, and the set of contacts with vias.

1 25. The memory card of claim 22 further comprising a cover extending over the first  
2 face and edges of the circuit board.

1 26. The memory card of claim 25 wherein the cover further extends over the second  
2 face of the circuit board, the cover having openings for the set of contacts.

1 27. A microprocessor controlled device comprising:

2 a memory chip package comprising a circuit board having a first and second face,  
3 a controller die attached to the first face, and a memory die attached to the second face;

4 one or more input-output devices;

5 random access memory; and

6 a microprocessor.

1 28. A memory chip package comprising:

2 a circuit board having first and second opposing faces;

3 a FLASH EEPROM having memory cells, the EEPROM attached to the first face  
4 of the circuit board;

5 a controller having a control logic, the controller attached to the second face of the  
6 circuit board and configured to read and write data to the memory cells on the first face;  
7 and

8 data lines connecting the controller die to the EEPROM and operable to transfer  
9 data to and from the memory cells.

1 29. The memory chip package of claim 28 wherein the controller further comprises:

2 a microprocessor;

3 a memory buffer; and

4 a system interface.

1 30. The memory chip package of claim 28 further comprising:

2 address lines connecting the memory cells on the first face to the controller on the  
3 second face, the address lines operable to address one or more memory cells for the  
4 reading and writing of the data.

1 31. The memory chip package of claim 30 further comprising:

2 control and status lines connecting the memory cells on the first face to the  
3 controller on the second face, the control and status lines operable to monitor the state of  
4 the memory cells over the control and status lines.

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